EV 313 842 011 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	REESE et al.	Confirmation No.:	To be assigned
Serial No.:	To be assigned	Art Unit:	To be assigned
Filed:	Herewith	Examiner:	To be assigned
For:	METHOD FOR IMPLEMENTING ELECTRO-STATIC DISCHARGE PROTECTION IN SILICON-ON-INSULATOR DEVICES	Attorney Docket No.:	9818-093-999

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of :

☒ Each U.S. patent application publication and U.S. and foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):
☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a or 3b)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $180.00 fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is:
☐ enclosed
☐ to be charged to Pennie & Edmonds LLP Deposit Account No. 16-1150.

(Item 3b to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

The $180.00 fee set forth in 37 C.F.R. §1.17(p) is:
☐ enclosed.
☐ to be charged to Pennie & Edmonds LLP Deposit Account No. 16-1150.

The Certification Statement in Item 5 below is applicable.

5. ☐ Certification Statement (applicable if Item 3a or Item 4 is checked)

(Check either Item 5a or 5b)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5c. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ This application is a continuation application under 37 C.F.R. §1.60 or §1.53(b) or (d).

(Check appropriate Items 6a, 6b and/or 6c)

6a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

6b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

6c. ☐ Copies of the publications listed on Form PTO-1449 were not previously cited in prior application Serial No. , filed on , and are provided herewith.

7. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 7a)

7a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

8. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 8a, 8b, or 8c)

8a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

8b. ☐ set forth in the application.

8c. ☐ enclosed as an attachment hereto.

9. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Pennie & Edmonds LLP Deposit Account No. 16-1150.

10. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: October 15, 2003

Francis E. Morris 24,615

Francis E. Morris (Reg. No.)

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LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)	ATTY DOCKET NO. 9818-093-999	APPLICATION NO To be assigned
	APPLICANT REESE et al.	
	FILING DATE Herewith	GROUP To be assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,811,857	09/22/1998	Assaderaghi et al.			
		6,034,397	03/07/2000	Voldman			
		6,404,269 B1	06/11/2002	Voldman			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Amerasekera et al., "ESD in Silicon Integrated Circuits", Second Edition, John Wiley & Sons, Ltd., 2002, pp. 200-206, 215-216
		Anderson and Krakauer, "ESD protection for mixed-voltage *I/O* using NMOS transistors stacked in a cascode configuration", Microelectronics Reliability, 39, 1999, pp. 1521-1529
		Duvvury et al., "ESD Design For Deep Submicron SOI Technology", Symposium on VLSI Technology Digest of Technical Papers, 1996, pp. 194-195
		Verhaege et al., "The ESD Protection Capability of SOI Snapback NMOSFETS: Mechanisms and Failure Modes", EOS/ESD Symposium, 1993, pp. 215-219
		Voldman et al., "Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors", EOS/ESD Symposium, 2000, pp. 239-250
		Voldman et al., "Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips", EOS/ESD Symposium, 1999, pp. 105-115
		Voldman et al., "Dynamic Threshold Body-and gate-coupled SOI ESD Protection Networks", Journal of Electrostatics, 44, 1998, pp. 239-255

EXAMINER	**DATE CONSIDERED**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.